at least one subinstruction, the processor comprising the plurality of clusters, each one cluster of the plurality of clusters comprising a plurality of functional processing units, the method comprising the steps of:

testing the set of control bits of the given instruction to identify a prescribed condition;

when the prescribed condition is identified, routing said subinstruction of the given instruction to multiple functional processing units as determined by the prescribed condition;

concurrently executing the subinstruction at said multiple functional processing units.

2. (Amended) The method of claim 1, in which the step of routing comprises routing said subinstruction of the given instruction to a first functional processing unit of a first cluster of the plurality of clusters and to a first functional processing unit of a second cluster of the plurality of clusters; and in which the step of executing comprises concurrently executing the subinstruction at said first functional processing unit of the first cluster of the plurality of clusters and at the first functional processing unit of the second cluster of the plurality of clusters.

4. (Amended) A method for storing an instruction of a computer program to be executed on a processor having a very long instruction word architecture,

wherein each instruction comprises at least one subinstruction and up to a first prescribed number of subinstructions, the first prescribed number being at least two,

wherein the processor is organized into a plurality of clusters equaling a second prescribed number, each one cluster of the plurality of clusters comprising a common number of functional processing units, wherein the common number of functional processing units times the second prescribed number equals the first prescribed number,

wherein for a given instruction having the first prescribed number of subinstructions, each functional processing unit of the plurality of clusters is for executing a respective subinstruction of the given instruction, the method comprising, during compilation of the computer program, the steps of:

identifying a pattern in which a subinstruction occurs more than once in the given instruction, said subinstruction being a redundant subinstruction;

determining whether the pattern is among a set of prescribed patterns;

when the pattern is among the set of prescribed patterns, setting a set of control bits for the instruction to indicate that said pattern is present.

5. (Amended) The method of claim 4, further comprising, during compilation of the computer program, compressing the given instruction when the pattern is among the set of prescribed patterns by deleting one occurrence of the redundant subinstruction in the given instruction to achieve a compressed instruction.

6. (Amended) The method of claim 5, further comprising, during run time of the computer program, the steps of:

moving the compressed instruction into an instruction cache;